AMENDMENTS TO THE SPECIFICATION

On page 6, line 8, please amend the corresponding paragraph as follows:

The edge detector 10, shown in Figure 3, consists simply of flip-flop 20 and an XOR gate 22 and outputs a "1" whenever a transition occurs in the input bit stream. The output of the edge detector register [[23]] is designated "G".

On page 6, line 27, please amend the corresponding paragraph as follows:

The NCO counter consists of three registers C_2, C_1 and C_0 (as shown in Figure 7), referred to collectively as "C". As graphically illustrated in Figure 5, the state transition diagram [[30]] 31 for C is derived from the following set of rules: